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| 09/388,857 | 09/01/1999 | LUAN C. TRAN | MI22-878 | 4528 |

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| ART UNIT | PAPER NUMBER |
| 2813 | 16 |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/388,857 | TRAN, LUAN C. | |
| | Examiner | Art Unit | |
| | Laura M Schillinger | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *03 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7 and 51-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 51-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *15* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 U.S.C. § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-7 and 51-73 are rejected under 35 U.S.C. 102(e) as being anticipated by Forbes ('351).

In reference to claim 1, Forbes teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the shallow trench isolation regions being formed to define a plurality of active areas, with some widths being no greater than 1 um, at least two of the widths being different (Fig.3 and Col.7, lines: 55-63);

forming a transistor gate line (wordline)over the active areas (Fig.4I (440) and Col.8, lines: 10-20), the transistor having different widths and voltages (Col.8, lines: 40-50).

### *Response to Arguments*

Applicant's arguments filed 12/7/01have been fully considered but they are not persuasive. Applicant argues that Forbes fails to teach a plurality of active areas. Applicant has made this argument in prior submissions- however it is incorrect- a doped N or P region results in formation of an active region- it is clearly depicted in Figure 3 that there are multiple active regions formed throughout the substrate. Furthermore, (defeating applicant's second argument with regards to the inapplicability of Col.7's disclosure to the active areas of Fig. 3), Col.7, lines:60-61 states: "these active areas 300 is approximately one square micron or less...". Active area 300 is SHOWN in Figure 3- and the disclosure of column 7 explicitly teaches that the width is that claimed by the applicant. Note further the "s" at the end of the term "area"- this plurality designation tells one of ordinary skill in the art that there is more than one active area- thus anticipating the "plurality of active areas" as recited by the applicant's claims. Applicant is further referred to Fig.s 4D showing active areas 300 and their respective trenches 402. Applicant argues that the passage reciting multiple active areas 300 are meant to disclose multiple wafers, however failed to cite support for this contention and the Examiner could not find such support for this interpretation in Forbes.

Applicant argues that Forbes fails to teach a plurality of active areas- howeveras cited by the Examiner, Col.7, lines: 55-63 explicitly state "active areas"- in the plural sense. Applicant argues that Col.7 does not describe Fig.3- but it describes layer 300 (the active areas)- found in Fig.3.

Applicant argues that Forbes teaches LOCOS isolation rather than trench isolation and refers to Col.7, lines: 55-63 as teaching that LOCOS isolates the active region. Examiner has reviewed the entire Forbes reference and cannot find where LOCOS is used to isolate the active region. Examiner has found trench isolation, but not LOCOS isolation (Abs., lines:15-17). The LOCOS process described in Col.7 acts to adjust the width of the active layer, making it wider or narrower- thus the phrase used by Forbes "defining the active area". This LOCOS process would also cause variations in the active regions width- and does not perform an isolation function rather the trenches perform this function. (Abs., lines:15-17)

*Applicant argues that Forbes fails to teach "shallow trench isolation", this inference means that Applicant argues that Forbes teaches only the formation of deep trenches. However, Forbes teaches "..in the memory cell of the invention, there are no stacked towers or DEEP TRENCHES.." (Col.11, lines: 29-30). Forbes explicitly teaches "trench isolation". Col.6, lines: 35-45 teaches that the depth of the trenches may equal to one micron or less (the width of the silicon bars). Wolf (the art cited by applicant to explain shallow trench isolation) teaches forming shallow trenches at a range between .3-.5 microns. Since Forbes teaches that the trenches may be less than one micron- it follows that Forbes does in fact teach shallow trench isolation. Furthermore, there is no obviousness issue present.* –stated by the Examiner, in the Examiner's final office action.

Applicant is misconstruing the Examiner's above arguments to suggest that the Examiner should be making a 103 rejection, by incorporating Wolf's teachings to show what depth

constitutes "shallow" as known in the art. This is not so, the Examiner was merely attempting to explain to the applicant the difference between Shallow/Moderate and Deep trench isolation. The Examiner infers that applicant realizes trench isolation structures are formed- applicant has claimed shallow and Forbes teaches that the trenches are shallow (Col.6, lines: 35-45).

In the response to Arguments made by the Examiner in her Final Office Action, the Examiner did not understand (as she does now by applicant's newly submitted arguments) that Applicant was arguing that NO shallow trench isolation exists at all. The Examiner completely disagrees, applicant argues that no shallow trench isolation exists on 2 grounds: 1) Forbes fails to explicitly use the term "shallow trench isolation" and 2) the shallow trench isolation process as described by Wolf is not taught in the Forbes reference. Applicant is incorrect- starting with argument 2: Wolf teaches forming the trench and refilling the trench with an oxide to form isolation regions- Forbes teaches the exact same process of forming and refilling the trenches with an oxide- Col.7, lines:48-56 describes refilling the shallow trenches. With respect to #1 argument made by applicant, although applicant is correct that Forbes does not call the process he describes "shallow trench isolation", he does refer to the trench as an "isolation trench"- Abs., lines: 15-17 furthermore he teaches etching the trenches to a depth which constitutes SHALLOW as defined in the art, and coincides with the meaning of "shallow" within the phrase "shallow trench isolation". "Shallow" is referring to the trench depth. This means that FORBES DOES TEACH shallow trench isolation. Examiner rejects applicant's claim based on Forbes because he describes his process as forming an "isolation trench", and further describes etching the isolating trenches to a shallow depth. Examiner does not believe that this constitutes giving the

term shallow trench isolation a meaning repugnant to the usual meaning of the term as applicant asserts. Forbes teaches to form isolating trenches at shallow depths and refilling them with oxide as understood by those of ordinary skill in the art to constitute "shallow trench isolation" and furthermore as described in scientific literature.

In reference to claim 2, Forbes teaches wherein there is no separate channel implant (Col.7-8, lines: 64-14).

In reference to claim 3, Forbes teaches wherein the widths are less than one micron (Col.7, lines: 55-63).

In reference to claim 4, Forbes teaches wherein the threshold voltages are less than 2 volts (Col.10, lines: 35-65).

In reference to claim 5, Forbes teaches wherein the threshold voltages are less than one volt (Col.10, lines: 35-65).

In reference to claim 6, Forbes teaches wherein the widths are less than one micron and the threshold voltages are less than 2 v (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 7, Forbes teaches wherein the widths are less than one micron and the threshold voltages are less than 1 v (Col.7, lines: 55-63 and Col.10, lines: 35-65)..

In reference to claim 51,Forbes teaches wherein one active area width is less than 1 um (Col.7, lines: 55-63).

In reference to claim 54, Forbes teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being less than 1 um , at least two being different (Col.7, lines: 55-63);

forming a transistor gate line over the active areas (Fig.4I (440) and Col.8, lines: 10-20), the transistor having different widths and voltages (Col.8, lines: 40-50).

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 55, Forbes teaches wherein the higher TV has an active area greater than 1 um (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 56, Forbes teaches wherein the higher TV has an active area less than 1 um (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 57, Forbes teaches wherein one common channel implant is conducted (Col.7-8, lines: 64-14).

In reference to claim 58, Forbes teaches wherein the gate line comprises a common gate line formed over the active areas (Fig.4I (440) and Col.8, lines: 10-20).

In reference to claim 59, Forbes teaches wherein the gate line comprises a common gate line and the Ts are parallel (Fig.4I (440) and Col.8, lines: 10-20).

In reference to claim 60, Forbes teaches wherein the TV are less than 1 V(Col.10, lines: 35-65).

In reference to claim 61, Forbes teaches wherein the widths are less than 1 um, and the TV are less than 2 V (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 62, Forbes teaches wherein the widths are less than 1um and the TV are less than 1 V (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 63, Forbes teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being less than 1 um, at least two being different (Fig. 3 and Col.7, lines: 55-63);

forming a transistor gate line over the active areas, the transistor having different widths and voltages less than 2 V (Col.7, lines: 55-63 and Col.10, lines: 35-65)., no channel implant (Col.7-8, lines: 64-14); and

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 64, Forbes teaches wherein the two widths are less than 1 um (Col.7, lines: 55-63).

In reference to claim 65, Forbes teaches wherein the TV are less than 1 v (Col.10, lines: 35-65)..

In reference to claim 66 Forbes teaches wherein the two widths are less than 1 um, and TVs are less than 1 v (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 67, Forbes teaches a method comprising:

forming a plurality of shallow trench isolation regions received within a substrate, the regions define active areas, with some widths being less than 1 um , at least two being different (Col.7, lines: 55-63);

forming a gate line over the active areas (Fig.4I (440) and Col.8, lines: 10-20), the transistor having different widths and voltages (Col.8, lines: 40-50) wherein the gate line comprises a common gate line and the Ts are parallel (Fig.4I (440) and Col.8, lines: 10-20)..

wherein the transistor with a lower threshold voltage has an active area with less than 1 um width (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 68, Forbes teaches wherein the higher TV has an active area greater than 1 um (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 69, Forbes teaches wherein the higher TV has an active area less than 1 um (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 70, Forbes teaches wherein one common channel implant is conducted (Col.7-8, lines: 64-14).

In reference to claim 71, Forbes teaches wherein the gate line comprises a common gate line formed over the active areas (Fig.4I (440) and Col.8, lines: 10-20).

In reference to claim 72, Forbes teaches wherein the two widths are less than 1 um, and TVs are less than 1 v (Col.7, lines: 55-63 and Col.10, lines: 35-65).

In reference to claim 73, Forbes teaches wherein the threshold voltages are less than 2 volts (Col.10, lines: 35-65).

***Claim Rejections - 35 U.S.C. § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes ('351).

In reference to claim 52, 53, and 74 are Forbes fails to explicitly teach forming 3 transistors each have a different threshold voltage. However, it would have been obvious to one of ordinary skill in the art to fabricate additional transistors in order to create additional read/write capabilities for the memory cell which function the same way disclosed by Forbes.

***Conclusion***

5. Any inquiry concerning this communication from examiner should be directed to Laura Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached by telephone on Monday to Friday from 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers, can be reached on (703) 308-2417. The fax phone number for the group is (703) 308-7722.

LMS

June 25, 2002

OLIK CHAUDHURI
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